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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,317	MARIAUD ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 5-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 5-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the request filed on 1st of March 2006 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/989,317, which the request is acceptable and an RCE has been established. Claims 5, 11, 17, 20, and 22 have been amended; no claim has been canceled; and no claim has been newly added since the RCE Final Office Action was mailed on 1st of November 2005. Currently, claims 5-22 are pending in this Application.

Claim Objections

2. Claims 5, 11, 17, and 20 are objected to because of the following informalities:

The claims 5, 11, 17, and 20 recite the two different subject matters "an interruption signal" in lines 19 and 21-22 of the claim 5, in lines 18-20 of the claim 11, in lines 15-16 and 18 of the claim 17, and in lines 14 and 16 of the claim 20, respectively. However, they recall the subject matter "the interruption signal" without designating which one of the two different subject matters "an interruption signal," respectively. Therefore, they fail to clearly point out which one of the two different subject matters "an interruption signal" is the antecedent basis of the subject matter "the interruption signal" in the respective claims 5, 11, 17, and 20, and then they make the claims 5, 11, 17, and 20 be indefinite, respectively. The Examiner presumes that the term "an interruption signal" in lines 21-22 of the claim 5, in lines 19-20 of the claim 11, in line 18 of the claim 17, and in line 16 of the claim 20, might be considered as --the interruption signal-- in light of the specification, respectively.

The claims 20 and 22 recite the subject matter "the microprocessor interruption signal" in line 21, respectively. However, it has not been specifically clarified in the claims 20 and 22. Therefore, the Examiner presumes that the term "the microprocessor interruption signal" could be considered as --the interruption signal-- in light of the specification since it is not defined in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 20 and 21 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for supplying an interruption signal when said sending/receiving circuit has received the start of a new message after the start of said new message has been acknowledged and recorded by said sending/receiving circuit (See Application, page 16, lines 25-28 and page 6, lines 12-15), does not reasonably provide enablement for supplying an interruption signal to a microprocessor of the slave apparatus once the start of a new message has been acknowledged and recorded by the sending/receiving circuit when the interruption signal is supplied (See Claim 20, lines 16-21 and Claim Objection on the Claim 20). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make/use the invention commensurate in scope with these claims.

In fact, the sending/receiving circuit supplies said interruption signal to the microprocessor of the slave apparatus once the start of a new message has been acknowledged and recorded by the sending/receiving circuit (See Application, page 5, lines 1-5). However, the Examiner doubts how the sending/receiving circuit in the claimed invention supplies said interruption signal to the microprocessor of the slave apparatus once the start of a new message has been acknowledged and recorded by the sending/receiving circuit when said interruption signal is supplied, which is causing a deadlock condition. In other words, *the start of a new message* has been acknowledged and recorded by the sending/receiving circuit when the interruption signal is supplied, however, the supplying interruption signal to the microprocessor **has not been** performed **before** *the start of a new message* has been acknowledged and recorded by the sending/receiving circuit. Therefore, the claim 20 is rejected under 35 U.S.C. 112, first paragraph (scope enablement issue), and the claim 21 is a dependent claim of the claim 20.

The Examiner presumes that the limitation "supplying an interruption signal to a microprocessor ... by the sending/receiving circuit when the interruption signal is supplied" could be considered as --supplying

an interruption signal to a microprocessor ... by the sending/receiving circuit-- in light of the specification and for the purpose of claim rejection under a prior art.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 5-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art [hereinafter AAPA] in view of Lee [US 6,256,699 B1].

Referring to claim 5, AAPA discloses a computer system (See Fig. 1) comprising:

- a master apparatus (i.e., Master Apparatus A in Fig. 1); and
- a slave apparatus (i.e., Slave Apparatus B in Fig. 1) for communicating with said master apparatus (See page 1, lines 10-22) and communicating via a universal serial bus (USB) protocol (See page 1, lines 22-25), said slave apparatus (i.e., said Slave Apparatus B) comprising
  - a sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) for sending and receiving binary information to and from said master apparatus (See page 1, line 25

through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3*),

- a plurality of state latches (e.g., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) and control circuitry (e.g., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) cooperating therewith for receiving said status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon (See page 7, line 18 through page 8, line 7†),
- a microprocessor (i.e., Microcontroller 28 of Fig. 1) for processing applications of said slave apparatus (See page 2, lines 8-13; i.e., wherein in fact that the microcontroller of the slave apparatus has to perform more and more tasks inherently anticipates a processor for processing applications of said slave apparatus) and also for processing said binary information received by said sending/receiving circuit (See page 3, lines 14-26; i.e., wherein in fact that an interruption of the microcontroller to process the part of the transmitted message may be requested inherently anticipates a processor for processing said binary information received by said sending/receiving circuit), and
- an interruption state latch and a control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) cooperating therewith for supplying an interruption signal (i.e., an interruption when said flag CTR is set to the logic 1 in Fig. 3(d)) to said microprocessor (See page 3, lines 14-20; i.e., wherein in fact that an interruption of said Microcontroller being requested by USB bus anticipates said interruption signal, viz., interruption request when CTR is set to logic 1 in Fig. 3(d), being supplied to said microprocessor).

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* See the specification pages 2-3, Background of the Invention.

† See the specification page 6, line 33 through page 8, line 7, the Applicants admit the portion as a prior art, i.e., the statement "about the existing system", and the prior responses have not argued with this admittance in the record.

AAPA does not teach that said microprocessor processing said binary information received by said sending/receiving circuit when the interruption signal is supplied; the interruption signal being supplied once the start of a new message has been acknowledged and recorded by said sending/receiving circuit; and said sending/receiving circuit also acknowledging the start of a following message while the interruption signal is supplied.

Lee discloses a reliable interruption reception over buffered bus (See Abstract), wherein

- a microprocessor (i.e., Host Processor 28 of Fig. 6) processing binary information (i.e., data) received by a sending/receiving circuit (i.e., Bridge with buffering 32 and Host Memory 30 in Fig. 6) when an interruption signal (i.e., processor alerting signal from Mailbox Register 62 to Interrupt Logic 66 in Fig. 6) is supplied (See col. 6, lines 41-51);
- the interruption signal (i.e., said processor alerting signal) being supplied once the start of a new message has been acknowledged (i.e., acknowledging the completion of transmitting said data by initiating device in Box 74 of Fig. 7) and recorded by said sending/receiving circuit (i.e., stored in target device, i.e., said Host Memory, through said Bridge with buffering in Box 74 of Fig. 7; See col. 5, lines 31-40); and
- said sending/receiving circuit (i.e., said Bridge with buffering and Host Memory) also acknowledging the start of a following message while the interruption signal is supplied (See col. 4, lines 58-61 and col. 5, lines 9-17; i.e., wherein in fact that a system having a buffered transaction bus and data being written first to host memory using a posted write inherently implies said sending/receiving circuit acknowledging the start of a following message while the interruption signal is supplied).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said reliable interruption reception mechanism, as disclosed by Lee, in said slave apparatus, as disclosed by AAPA, so as to cooperate said reliable interruption reception mechanism with

said interruption state latch and said control circuit, for the advantage of assuring that said binary information (i.e., data) is waiting in said sending/receiving circuit (i.e., host memory) before said microprocessor (i.e., host processor) receives said interruption signal (i.e., interrupt request; See Lee, col. 5, line 62 through col. 6, line 3).

Referring to claim 6, AAPA teaches said control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) for controlling said interruption state latch (See page 3, lines 14-26) comprises

- at least one logic circuit (i.e., means for switching/latching signals between "1" and "0" for Setup, CTR and End_trans signals in Fig. 3) for receiving said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) from said sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) and setting said interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic 1 state) to indicate a microprocessor interruption request (See page 3, lines 14-18).

Referring to claim 7, AAPA teaches

- said control circuitry (i.e., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) for controlling said state latches (i.e., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) prevents said binary information from said sending/receiving circuit (i.e., message from Master Apparatus via Send/Receive device; See page 1, line 25 through page 2, line 3) from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal (See phases 12 and 14 in Fig. 3, and page 3, lines 14-29; i.e., wherein in fact that no transfer over the USB bus is authorized during CTR being set to '1' inherently anticipates said control circuitry prevents the binary information

from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal).

Referring to claim 8, AAPA teaches

- said master apparatus (i.e., Master Apparatus A in Fig. 1) comprises a central processing unit (i.e., Microcontroller 26 of Fig. 1).

Referring to claim 9, AAPA teaches

- said slave apparatus (i.e., Slave Apparatus B in Fig. 1) comprises computer peripheral device (See page 1, line 3-5).

Referring to claim 10, AAPA teaches

- a cable (i.e., cable 20 of Fig. 1) connecting said master apparatus and said slave apparatus (See page 1, lines 10-19).

Referring to claim 11, AAPA discloses a computer system (See Fig. 1) comprising:

- a master apparatus (i.e., Master Apparatus A in Fig. 1); and
- a slave apparatus (i.e., Slave Apparatus B in Fig. 1) for communicating with said master apparatus (See page 1, lines 10-22) and comprising
  - a sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) for sending and receiving binary information to and from said master apparatus (See page 1, line 25 through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3),

- a plurality of state latches (e.g., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) and control circuitry (e.g., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) cooperating therewith for receiving said status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon (See page 7, line 18 through page 8, line 7),
- a microprocessor (i.e., Microcontroller 28 of Fig. 1) for processing applications of said slave apparatus (See page 2, lines 8-13; i.e., wherein in fact that the microcontroller of the slave apparatus has to perform more and more tasks inherently anticipates a processor for processing applications of said slave apparatus) and also for processing said binary information received by said sending/receiving circuit (See page 3, lines 14-26; i.e., wherein in fact that an interruption of the microcontroller to process the part of the transmitted message may be requested inherently anticipates a processor for processing said binary information received by said sending/receiving circuit),
- an interruption state latch (i.e., a flag CTR in Fig. 3(d)) for supplying an interruption signal (i.e., an interruption when CTR is set to the logic 1 in Fig. 3(d)) to said microprocessor (See page 3, lines 14-20; i.e., wherein in fact that an interruption of said Microcontroller being requested by USB bus clearly anticipates said interruption signal, viz., interruption request when CTR is set to the logic 1 in Fig. 3(d), being supplied to said microprocessor), and
- said control circuitry (i.e., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) for controlling said state latches (i.e., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) preventing said binary information from said sending/receiving circuit (i.e., message from Master Apparatus via Send/Receive device; See page 1, line 25 through page 2, line 3) from being written into said plurality

of state latches during receipt of the start of said new message and during the presence of said interruption signal (See phases 12 and 14 in Fig. 3, and page 3, lines 14-29; i.e., wherein in fact that no transfer over the USB bus is authorized during CTR being set to the logic 1 inherently anticipates said control circuitry prevents the binary information from being written into said plurality of state latches during receipt of said start of said new message and during the presence of said interruption signal).

AAPA does not teach that said microprocessor processing said binary information received by said sending/receiving circuit when the interruption signal is supplied; the interruption signal being supplied once the start of a new message has been acknowledged and recorded by said sending/receiving circuit; and said sending/receiving circuit also acknowledging the start of a following message while the interruption signal is supplied.

Lee discloses a reliable interruption reception over buffered bus (See Abstract), wherein

- a microprocessor (i.e., Host Processor 28 of Fig. 6) processing binary information (i.e., data) received by a sending/receiving circuit (i.e., Bridge with buffering 32 and Host Memory 30 in Fig. 6) when an interruption signal (i.e., processor alerting signal from Mailbox Register 62 to Interrupt Logic 66 in Fig. 6) is supplied (See col. 6, lines 41-51);
- the interruption signal (i.e., said processor alerting signal) being supplied once the start of a new message has been acknowledged (i.e., acknowledging the completion of transmitting said data by initiating device in Box 74 of Fig. 7) and recorded by said sending/receiving circuit (i.e., stored in target device, i.e., said Host Memory, through said Bridge with buffering in Box 74 of Fig. 7; See col. 5, lines 31-40); and
- said sending/receiving circuit (i.e., said Bridge with buffering and Host Memory) also acknowledging the start of a following message while the interruption signal is supplied (See col. 4, lines 58-61 and col. 5, lines 9-17; i.e., wherein in fact that a system having a buffered

transaction bus and data being written first to host memory using a posted write inherently implies said sending/receiving circuit acknowledging the start of a following message while the interruption signal is supplied).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said reliable interruption reception mechanism, as disclosed by Lee, in said slave apparatus, as disclosed by AAPA, so as to cooperate said reliable interruption reception mechanism with said interruption state latch and said control circuit, for the advantage of assuring that said binary information (i.e., data) is waiting in said sending/receiving circuit (i.e., host memory) before said microprocessor (i.e., host processor) receives said interruption signal (i.e., interrupt request; See Lee, col. 5, line 62 through col. 6, line 3).

Referring to claim 12, AAPA teaches

- said master apparatus and said slave apparatus communicate via a universal serial bus (USB) protocol (See page 1, lines 22-25).

Referring to claim 13, AAPA teaches

- at least one logic circuit (i.e., means for switching/latching signals between "1" and "0" for Setup, CTR and End_trans signals in Fig. 3) for receiving said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) from said sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) and setting said interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic 1 state) to indicate a microprocessor interruption request (See page 3, lines 14-18).

Referring to claim 14, AAPA teaches

- said master apparatus (i.e., Master Apparatus A in Fig. 1) comprises a central processing unit (i.e., Microcontroller 26 of Fig. 1).

Referring to claim 15, AAPA teaches

- said slave apparatus (i.e., Slave Apparatus B in Fig. 1) comprises computer peripheral device (See page 1, line 3-5).

Referring to claim 16, AAPA teaches

- a cable (i.e., cable 20 of Fig. 1) connecting said master apparatus and said slave apparatus (See page 1, lines 10-19).

Referring to claim 17, AAPA discloses a slave apparatus (i.e., Slave Apparatus B in Fig. 1) for communicating with a master apparatus (i.e., Master Apparatus A in Fig. 1; See page 1, lines 10-22) via a universal serial bus (USB) protocol (See page 1, lines 22-25), said slave apparatus comprising:

- a sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) for sending and receiving binary information to and from said master apparatus (See page 1, line 25 through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3);
- a plurality of state latches (e.g., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) and control circuitry (e.g., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) cooperating therewith for receiving said status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon (See page 7, line 18 through page 8, line 7);

- a microprocessor (i.e., Microcontroller 28 of Fig. 1) for processing applications of said slave apparatus (See page 2, lines 8-13; i.e., wherein in fact that the microcontroller of the slave apparatus has to perform more and more tasks inherently anticipates a processor for processing applications of said slave apparatus) and also for processing said binary information received by said sending/receiving circuit (See page 3, lines 14-26; i.e., wherein in fact that an interruption of the microcontroller to process the part of the transmitted message may be requested inherently anticipates a processor for processing said binary information received by said sending/receiving circuit); and
- an interruption state latch (i.e., a flag CTR in Fig. 3(d)) and a control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) cooperating therewith for supplying an interruption signal (i.e., an interruption when CTR is set to '1' in Fig. 3(d)) to said microprocessor (See page 3, lines 14-20; i.e., wherein in fact that an interruption of said Microcontroller being requested by USB bus clearly anticipates said interruption signal, viz., interruption request when CTR is set to '1' in Fig. 3(d), being supplied to said microprocessor) once the end of a message has been acknowledged and for supplying the transfer interruption signal to said microprocessor (i.e., said flag CTR is the logic 1; See page 3, lines 14-20) once the start of a new message (e.g., message including SETUP and DATA in the phase 10 of Fig. 3(a)) has been acknowledged and recorded by said sending/receiving circuit (i.e., said CTR being set to the logic 1 after ACK in the phase 10 of Fig. 3(a); See page 3, lines 14-20; i.e., said interruption is supplied for processing the part of the transmitted message).

AAPA does not teach that said microprocessor processing said binary information received by said sending/receiving circuit when the interruption signal is supplied; the interruption signal being supplied once the start of a new message has been acknowledged and recorded by said sending/receiving circuit;

and said sending/receiving circuit also acknowledging the start of a following message while the interruption signal is supplied.

Lee discloses a reliable interruption reception over buffered bus (See Abstract), wherein

- a microprocessor (i.e., Host Processor 28 of Fig. 6) processing binary information (i.e., data) received by a sending/receiving circuit (i.e., Bridge with buffering 32 and Host Memory 30 in Fig. 6) when an interruption signal (i.e., processor alerting signal from Mailbox Register 62 to Interrupt Logic 66 in Fig. 6) is supplied (See col. 6, lines 41-51);
- the interruption signal (i.e., said processor alerting signal) being supplied once the start of a new message has been acknowledged (i.e., acknowledging the completion of transmitting said data by initiating device in Box 74 of Fig. 7) and recorded by said sending/receiving circuit (i.e., stored in target device, i.e., said Host Memory, through said Bridge with buffering in Box 74 of Fig. 7; See col. 5, lines 31-40); and
- said sending/receiving circuit (i.e., said Bridge with buffering and Host Memory) also acknowledging the start of a following message while the interruption signal is supplied (See col. 4, lines 58-61 and col. 5, lines 9-17; i.e., wherein in fact that a system having a buffered transaction bus and data being written first to host memory using a posted write inherently implies said sending/receiving circuit acknowledging the start of a following message while the interruption signal is supplied).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said reliable interruption reception mechanism, as disclosed by Lee, in said slave apparatus, as disclosed by AAPA, so as to cooperate said reliable interruption reception mechanism with said interruption state latch and said control circuit, for the advantage of assuring that said binary information (i.e., data) is waiting in said sending/receiving circuit (i.e., host memory) before said

microprocessor (i.e., host processor) receives said interruption signal (i.e., interrupt request; See Lee, col. 5, line 62 through col. 6, line 3).

Referring to claim 18, AAPA teaches said control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) for controlling said interruption state latch (See page 3, lines 14-26) comprises

- at least one logic circuit (i.e., means for switching/latching signals between "1" and "0" for Setup, CTR and End_trans signals in Fig. 3) for receiving said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) from said sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) and setting said interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic '1' state) to indicate a microprocessor interruption request (See page 3, lines 14-18).

Referring to claim 19, AAPA teaches

- said control circuitry (i.e., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) for controlling said state latches (i.e., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) prevents said binary information from said sending/receiving circuit (i.e., message from Master Apparatus via Send/Receive device; See page 1, line 25 through page 2, line 3) from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal (See phases 12 and 14 in Fig. 3, and page 3, lines 14-29; i.e., wherein in fact that no transfer over the USB bus is authorized during CTR being set to '1' inherently anticipates said control circuitry prevents the binary information from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal).

Referring to claim 20. AAPA discloses a method of processing interruptions (See page 3, lines 14-26) in a slave apparatus (i.e., Slave Apparatus B in Fig. 1) communicating with a master apparatus (i.e., Master Apparatus A in Fig. 1) via a universal serial bus (USB) protocol (See page 1, lines 22-25), said method comprising:

- sending and receiving binary information to and from said master apparatus via a sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1; See page 1, line 25 through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3);
- generating state signals of said sending/receiving circuit based upon said status signals (See page 7, line 18 through page 8, line 7);
- processing applications of said slave apparatus (i.e., SW Process 'main routine' in Fig. 3(e)) and also processing said binary information received by said sending/receiving circuit (See page 3, lines 24-26); and
- supplying an interruption signal (i.e., CTR being set to '1' in Fig. 3(d)) to a microprocessor of said slave apparatus (i.e., Microcontroller 28 of said Slave Apparatus B in Fig. 1; See page 3, lines 14-20, wherein in fact that an interruption of said Microcontroller being requested by USB bus clearly anticipates said interruption signal, viz., interruption request when CTR is set to '1' in Fig. 3(d), being supplied to said microprocessor).

AAPA does not teach that said processing said binary information is performed when the interruption signal is supplied; said supplying said interruption signal is performed once the start of a new message has been acknowledged and recorded by said sending/receiving circuit; and sending an acknowledgment from the sending/receiving circuit to the master apparatus acknowledging the start of a following message while the interruption signal is supplied.

Lee discloses a reliable interruption reception over buffered bus (See Abstract), wherein

- processing binary information (i.e., data) received by a sending/receiving circuit (i.e., Bridge with buffering 32 and Host Memory 30 in Fig. 6) when an interruption signal (i.e., processor alerting signal from Mailbox Register 62 to Interrupt Logic 66 in Fig. 6) is supplied (See col. 6, lines 41-51);
- supplying the interruption signal (i.e., said processor alerting signal) once the start of a new message has been acknowledged (i.e., acknowledging the completion of transmitting said data by initiating device in Box 74 of Fig. 7) and recorded by said sending/receiving circuit (i.e., stored in target device, i.e., said Host Memory, through said Bridge with buffering in Box 74 of Fig. 7; See col. 5, lines 31-40); and
- sending an acknowledgment from the sending/receiving circuit (i.e., responding to the interrupt by host process via mail box register, in fact, via said Bridge with buffering) to the master apparatus (i.e., to the initiator; See col. 5, lines 53-55) acknowledging the start of a following message while the interruption signal is supplied (See col. 4, lines 58-61 and col. 5, lines 9-17; i.e., wherein in fact that a system having a buffered transaction bus, responding to the interrupt by host process via mail box register, and data being written first to host memory using a posted write, inherently implies said sending/receiving circuit acknowledging the start of a following message while the interruption signal is supplied).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said reliable interruption reception mechanism, as disclosed by Lee, in said method of processing interruptions in said slave apparatus, as disclosed by AAPA, so as to cooperate said reliable interruption reception mechanism with said method of processing interruptions in said slave apparatus, for the advantage of assuring that said binary information (i.e., data) is waiting in said

sending/receiving circuit (i.e., host memory) before said microprocessor (i.e., host processor) receives said interruption signal (i.e., interrupt request; See Lee, col. 5, line 62 through col. 6, line 3).

Referring to claim 21, AAPA teaches

- supplying said interruption signal comprises setting an interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic '1' state) based upon said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) to indicate a microprocessor interruption request (See page 3, lines 14-18).

Referring to claim 22, AAPA discloses a method of processing interruptions (See page 3, lines 14-26) in a slave apparatus (i.e., Slave Apparatus B in Fig. 1) communicating with a master apparatus (i.e., Master Apparatus A in Fig. 1) via a universal serial bus (USB) protocol (See page 1, lines 22-25), said method comprising:

- generating a state signal indicating the end of a message (See page 1, line 26 through page 2, line 6);
- detecting a start of a new message (i.e., message 'IN' signal in Fig. 3(a)) from said master apparatus (See page 2, lines 7-10) and producing a start of message state signal (i.e., 'ready' state signal);
- acknowledging and recording said new message if a transfer interruption signal (i.e., a flag CTR) is not supplied (i.e., said flag CTR is the logic 0; See page 3, lines 20-29);
- supplying the transfer interruption signal to said microprocessor (i.e., said flag CTR is the logic 1; See page 3, lines 14-20) once the start of a new message (e.g., message including SETUP and DATA in the phase 10 of Fig. 3(a)) has been acknowledged and recorded (i.e., said CTR being set to the logic 1 after ACK in the phase 10 of Fig. 3(a));

- generating a signal (i.e., flag CTR in Fig. 3(d)) indicating completion (i.e., CTR being set to '0' in Fig. 3(d)) of recordation of said data from the start of said new message (See page 3, lines 14-26); and
- generating an interruption signal (i.e., an interruption when CTR is set to '1' in Fig. 3(d)) for a microprocessor of said slave apparatus (i.e., Microcontroller 28 of said Slave Apparatus B in Fig. 1; See page 3, lines 14-20, wherein in fact that an interruption of said Microcontroller being requested by USB bus clearly anticipates said interruption signal, viz., interruption request when CTR is set to '1' in Fig. 3(d), being supplied to said microprocessor) in the presence of said state signal indicating the end of said message, the start of message state signal, and said signal indicating completion of recordation of said data from the start of said new message when the interruption signal is supplied (See page 3, lines 14-20; i.e., wherein in fact that at the end of transfer phase, an interruption of the microcontroller to process the part of the transmitted message may be requested inherently anticipates generating an interruption signal in the presence of said state signal indicating the end of said message (i.e.. CTR being set to '1'). the start of message state signal (i.e., 'ready' state signal), and said signal indicating completion of recordation of said data from the start of said new message when the interruption signal is supplied).

AAPA does not teach that acknowledging the start of a following message while the interruption signal is supplied.

Lee discloses a reliable interruption reception over buffered bus (See Abstract). wherein

- generating an interruption signal (i.e., said processor alerting signal; See col. 5, lines 44-47); and
- acknowledging the start of a following message while the interruption signal is supplied (See col. 4, lines 58-61 and col. 5, lines 9-17; i.e., wherein in fact that a system having a buffered

transaction bus and data being written first to host memory using a posted write, inherently implies acknowledging the start of a following message while the interruption signal is supplied). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said reliable interruption reception mechanism, as disclosed by Lee, in said method of processing interruptions in said slave apparatus, as disclosed by AAPA, so as to cooperate said reliable interruption reception mechanism with said method of processing interruptions in said slave apparatus, for the advantage of assuring that said binary information (i.e., data) is waiting in said sending/receiving circuit (i.e., host memory) before said microprocessor (i.e., host processor) receives said interruption signal (i.e., interrupt request; See Lee, col. 5, line 62 through col. 6, line 3).

Response to Arguments

7. Applicants' arguments with respect to claims 5, 11, 17, 20, and 22 have been considered but are moot in view of the new ground(s) of rejection.

In fact, the Examiner brought Lee reference in the rejection for the limitations which are not provided by AAPA reference in the record because the Applicants' arguments were drawn from the newly amended limitations (See the Response on page 13 in particular).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fiacconi et al. [US 4,862,354] disclose multiprocessor system with interrupt notification and verification unit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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